AN-501

Application Note: Phase Synchronization

Applies to: *SSG4522ALX ,SSG4522ATLX*

Document Revision: 1.0

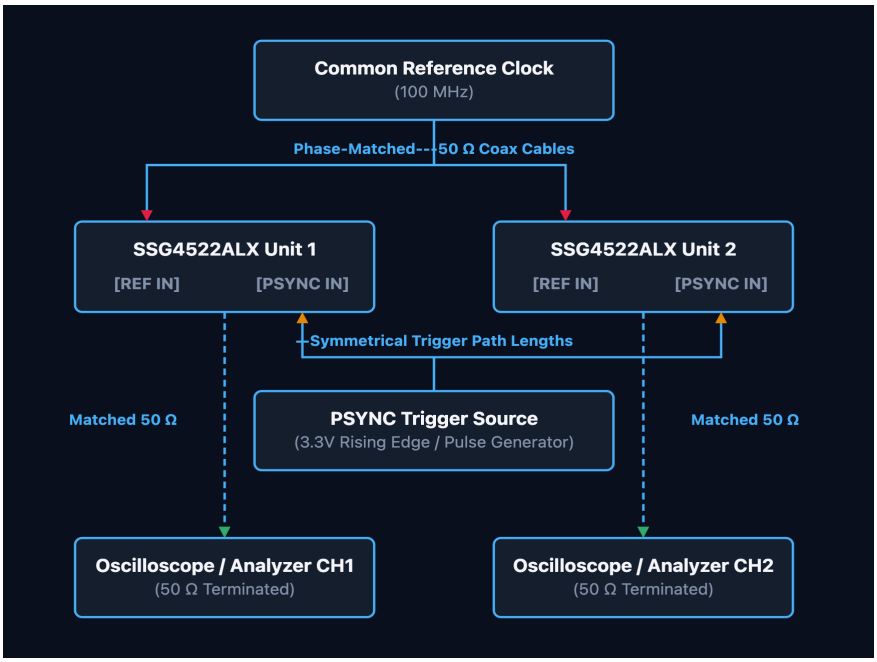
1. Overview

A variety of Z-Communication products support deterministic **Phase Synchronization** across their RF outputs (CH1 and CH2 if applicable) as well as across multiple connected units.

Every applicable unit is factory-programmed and delivered with internal synchronization registers active by default:

There is no need to configure register-level architecture. To engage phase alignment, users only need to provide the external reference clock and trigger the hardware **PSYNC** port according to the guidelines below.

2. Test Bench Setup & Critical Prerequisites



2.1 Symmetrical Path Matching

- **Master Reference Input:** Both RF channels/units must share the exact same external 100 MHz reference source split via a calibrated power divider/splitter.

- **Cable Matching:** Coaxial cable runs between the reference source, the PSYNC pulse line, and the measuring instrument must be **electrically length-matched phase-stable cables**.
- **50 Ω High-Frequency Termination:**
    - All RF outputs (CH1 and CH2) **must be terminated into clean 50 Ω loads** at the measurement instrument (oscilloscope, spectrum analyzer, or digitizer).
    - Leaving an unselected or inactive RF output open or improperly terminated will cause standing-wave reflections back into the synthesizer output stage, degrading phase tracking and output flatness.

2.2 DC Power Delivery

- Input supply voltage (V_{IN}) across units does not need to be identical. Any standard clean DC supply satisfying the unit's operating voltage specification ($\geq 5.0V$) is sufficient.

3. How to Engage & Trigger PSYNC

3.1 Trigger Input Specifications

- **Logic Level:** Nominal **3.3V CMOS** into the dedicated front/rear **PSYNC** port (active-high).
- **Pulse Shape:** A clean low-to-high step or pulse ($\geq 100ns$ width). A benchtop pulse generator, microcontroller GPIO, or lab power supply toggle can be used.

3.2 Trigger Sequencing Modes

Trigger PSYNC using either of two workflows:

- **Method A (Pre-Power Latching):** Apply 3.3V to the PSYNC port prior to powering on the SSG unit. When the unit boots and locks to the external reference, it immediately latches into phase alignment.
- **Method B (Live Latching):** With the SSG powered on and RF outputs active, assert a 3.3V rising edge into the PSYNC port. The output dividers will reset and latch into deterministic phase coherence.

3.3 How to Disengage / Reset Phase Sync

To return the device to its default, autonomous divider state:

1. Remove or ground the 3.3V signal on the PSYNC port.
2. **Power-cycle** the unit.

4. Operational Alignment & Channel Deskewing

Because internal channel dividers power up in arbitrary binary states, free-running channels will exhibit a random phase offset on every boot cycle. Asserting PSYNC eliminates this random state and locks the channels to a deterministic, repeatable relative phase. Below is PSYNC applied to different frequencies before and after the 3.3V rising edge is applied.

250 MHz:



PSYNC ON



PSYNC OFF

1000 MHz:

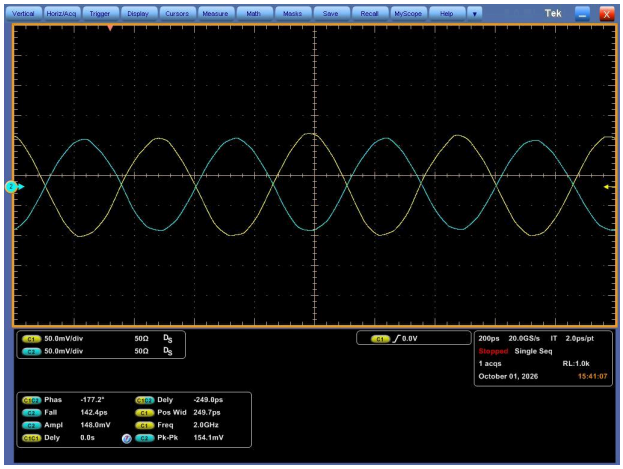


PSYNC ON

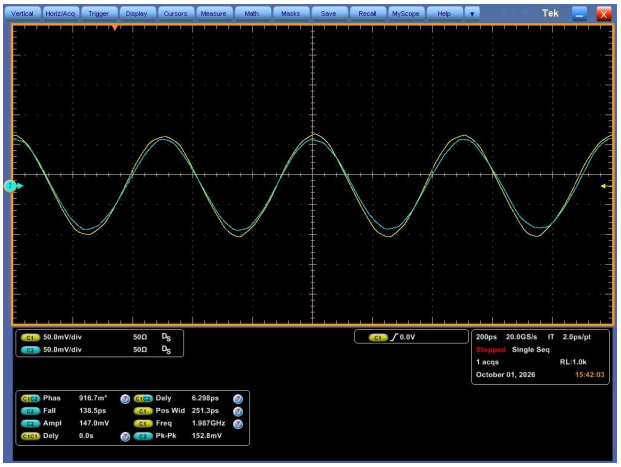


PSYNC OFF

2000 MHz:



PSYNC ON



PSYNC OFF

Calibrating / Deskewing CH1 and CH2:

1. Connect CH1 and CH2 to your oscilloscope using phase-matched 50 Ω cables and select **50 Ω DC input coupling** on all scope channels.
2. Assert the 3.3V PSYNC edge. Both channels should receive PSYNC within the same time window.
3. Observe both channels on the display. The phase relationship is now fixed and repeatable across any subsequent retuning or power cycles.
4. Any minor residual static phase offset observed at higher RF frequencies is predominantly due to external fixture/cable length tolerances. Apply the channel deskew feature on your oscilloscope or digital phase shifter to zero out the baseline offset.

5. Summary Checklist

Step	Action	Verification
1. Cabling	Connect master reference and RF outputs using matched 50 Ω lines.	Ensure scope/analyzer inputs are set to **50 Ω termination**.
2. Power	Supply $V_{IN} \geq 5.0V$ to all units.	Verify power and lock indicator LED is solid.

3. Trigger	Apply 3.3V rising edge to the **PSYNC** port.	Outputs will snap into fixed, deterministic phase alignment.
4. Calibrate	Zero out any residual cable delay on instrument channel deskew.	Phase remains coherent and locked across operations.