Recommended Reference Oscillator Output For:
SSG, FSG, SFS, Family Products

Output Power (Sine Wave): 0 dBm to +6 dBm (0.63 Vpp to 1.4 Vpp into 50 Ω).
This range ensures compatibility with all PLL chips while avoiding overdrive.

CMOS Output: Logic levels compatible with 3.3 V VDD (low < 0.4 V, high > 2.0 V) for direct interfacing.

Phase Noise: <-140 dBc/Hz @ 10 kHz offset to minimize in-band noise. (note1)
Harmonics/Spurs: <-60 dBc to avoid spurious tones.

Sine Wave vs. CMOS:
Use a sine wave oscillator (TCXO or OCXO) with AC coupling for lowest phase noise (note2).
If CMOS is needed, ensure fast rise/fall times (<5 ns) to avoid jitter.

note 1. The input reference signal should be 10 dB better than the noise floor of PLL+VCO to avoid degradation of the PLL noise contribution.
note2.for reference frequencies above 50 MHz
note3. For all SSG and FSG products 100 MHz reference is strongly recommended for best phase noise performance

Typical Reference Internal Circuit: